Amendment to the Claims:

The claims under examination in this application, including their current status and changes made in this paper, are respectfully presented.

Claims 1 – 2 (canceled).

3 (currently amended). The method of claim ~~1~~ 4 wherein the first error detection algorithm is a 1-bit error correction code (ECC) algorithm and the second error detection algorithm is a 2-bit ECC algorithm.

4 (currently amended). ~~The~~ A method ~~of claim 1 wherein the indicator has a value~~ for storing data within a non-volatile memory comprised of a plurality of blocks in an array formed on a semiconductor substrate, each of the plurality of blocks having an indicator indicative of whether the block is a reclaimed block, the method comprising:

identifying a first block of the plurality of blocks into which the data is to be stored;

responsive to the indicator associated with the first block meeting a criterion, encoding the data using a first error detection algorithm;

then writing the encoded data into the first block;

identifying a second block of the plurality of blocks into which data is to be stored;

responsive to the indicator associated with the second block not meeting the criterion, encoding the data using a second error detection algorithm, the second error detection algorithm having a higher error detection capability than the first error detection algorithm; and

then writing the encoded data into the second block.

5 (canceled).

6 (previously presented). A method for storing data within a non-volatile memory, comprised a plurality of blocks in an array formed on a semiconductor substrate, of a memory system, the method comprising:

identifying one of the plurality of blocks into which the data is to be stored;

obtaining an indicator associated with the identified block, the indicator having a value indicative of a number of times the first block has been erased;

determining whether the indicator is less than a threshold value,

responsive to the indicator being less than the threshold value, encoding the data using the first algorithm and then writing the data encoded using a first error detection algorithm into the identified block;

responsive to the indicator not being less than the threshold value, encoding the data using a second algorithm and then writing the data encoded using a second error detection algorithm into the identified block, the second error detection algorithm having a higher error detection capability than the first error detection algorithm;

repeating the identifying, obtaining, determining, encoding, and writing steps for another block in the array;

wherein, as a result of the repeating step, a first block in the array stores data encoded according to the first algorithm, and a second block in the array stores data encoded according to the second algorithm.

7 (currently amended). The method of claim ~~1~~ 6 wherein the indicator has a value indicative of an approximately average number of times blocks within the non-volatile memory have been erased.

8 (currently amended). The method of claim ~~1~~ 6 wherein the indicator is stored in a data structure, the data structure being substantially separate from the first block,

and wherein obtaining the indicator associated with the block includes obtaining the indicator from the data structure.

9 (currently amended). The method of claim ~~1~~ 6 wherein the non-volatile memory is a flash memory.

10 (original). The method of claim 9 wherein the flash memory is one of a NAND flash memory and an MLC NAND flash memory.

11 (currently amended). The method of claim ~~1~~ 6, further comprising:

identifying the first block as a block from which data is to be read;

obtaining the indicator associated with the first block;

responsive to the indicator associated with the first block meeting a criterion, decoding the data stored in the first block using the first error detection algorithm; and

responsive to the indicator associated with the first block not meeting the criterion, decoding the data using the second error detection algorithm.

12 (canceled).

13 (previously presented). The method of claim 11 wherein the first error detection algorithm is a 1-bit ECC algorithm and the second error detection algorithm is a 2-bit ECC algorithm.

Claims 14 – 15 (canceled).

16 (previously presented). A method for reading data within a non-volatile memory comprised of a plurality of blocks in an array formed on a semiconductor substrate, the method comprising:

identifying one of the plurality of blocks from which data is to be read;

obtaining an indicator associated with the identified block, the indicator having a value indicative of a number of times the identified block has been erased;

determining whether the indicator is less than a threshold value,

responsive to the indicator being less than the threshold value, decoding the data using a first error detection algorithm;

responsive to the indicator not being less than the threshold value, decoding the data using a second error detection algorithm, the second error detection algorithm having a higher error detection capability than the first error detection algorithm.

17 (previously presented). The method of claim 11 wherein the indicator has a value indicative of an approximately average number of times physical blocks of the non-volatile memory have been erased.

18 (previously presented). The method of claim 11 wherein the indicator is stored in a data structure, the data structure being substantially separate from the first block,

and wherein obtaining the indicator associated with the block includes obtaining the indicator from the data structure.

19 (original). The method of claim 11 wherein the non-volatile memory is a flash memory.

20 (original). The method of claim 19 wherein the flash memory is one of a NAND flash memory and an MLC NAND flash memory.

21 (currently amended). A memory system comprising:

a non-volatile memory array formed on a semiconductor substrate, the array including a plurality of blocks;

code devices for identifying a block into which data is to be stored;

code devices for obtaining an indicator associated with the identified block, the indicator having a value arranged to indicate whether the block is a reclaimed block ~~indicative of reliability of the identified block~~;

code devices for encoding the data using a first error detection algorithm responsive to the indicator meeting a criterion, and for encoding the data using a second error detection algorithm responsive to the indicator not meeting the criterion, the second error detection algorithm having a higher error detection capability than the first error detection algorithm;

code devices for writing encoded data into the identified block; and

a memory area that stores the code devices.

22 (canceled).

23 (previously presented). The memory system of claim 21 wherein the first error detection algorithm is a 1-bit ECC algorithm and the second error detection algorithm is a 2-bit ECC algorithm.

Claims 24 – 25 (canceled).

26 (previously presented). A memory system comprising:

a non-volatile memory array formed on a semiconductor substrate, the array including a plurality of blocks;

code devices for identifying a block into which data is to be stored;

code devices for obtaining an indicator associated with the identified block, the indicator having a value indicative of a number of times the identified block has been erased;

code devices for determining whether the indicator is less than a threshold value,

code devices for encoding the data using a first algorithm responsive to the indicator being less than the threshold value;

code devices for writing the data encoded using the first algorithm into the identified block;

code devices for encoding the data using a second algorithm responsive to determining that the data is not to be encoded using the first algorithm, the second error detection algorithm having a higher error detection capability than the first error detection algorithm;

code devices for writing the data encoded using the second algorithm into the identified block; and

a memory area that stores the code devices.

27 (original). The memory system of claim 21 wherein the non-volatile memory is one of a NAND flash memory and an MLC NAND flash memory.

28 (previously presented). The memory system of claim 21, further comprising:

code devices for determining whether the indicator meets the criterion;

code devices for decoding the data using the first error detection algorithm responsive to the indicator meeting the criterion, and for decoding the data using the second error detection algorithm responsive to the indicator not meeting the criterion.

29 (canceled).

30 (previously presented). The memory system of claim 28 wherein the first error detection algorithm is a 1-bit ECC algorithm and the second error detection algorithm is a 2-bit ECC algorithm.

31 (previously presented). The memory system of claim 28 wherein the indicator is arranged to indicate whether the block is a reclaimed block.

32 (previously presented). The memory system of claim 28 wherein the indicator ~~is~~ has a value indicative of a number of times the block has been erased.

33 (previously presented). A memory system comprising:

a non-volatile memory array formed on a semiconductor substrate, the array including a plurality of blocks, each including data;

code devices for identifying a block;

code devices for obtaining an indicator associated with the identified block, the indicator having a value indicative of a number of times the block has been erased;

code devices for determining whether the indicator is less than a threshold value,

code devices for decoding the data using a first error detection algorithm responsive to the indicator being less than the threshold value;

code devices for decoding the data using a second error detection algorithm responsive to the indicator not being less than the threshold value, the second error detection algorithm having a higher error detection capability than the first error detection algorithm; and

a memory area that stores the code devices.

34 (previously presented). The memory system of claim 28 wherein the non-volatile memory is one of a NAND flash memory and an MLC NAND flash memory.

Claims 35 – 45 (canceled).